

MI8380

**Intel Alder Lake-N (12th Gen Core CPU)
Mini-iTx SBC**

USER'S MANUAL

Version 1.0

AUGUST 2023

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Safety Information

Environmental conditions:

- Use this product in environments with ambient temperatures between 0°C and 60°C.
- Do not leave this product in an environment where the storage temperature may be below -20° C or above 80° C. To prevent from damages, the product must be used in a controlled environment.

Care for your products:

- Before cleaning the PCB, unplug all cables and remove the battery.
- Clean the PCB with a circuit board cleaner or degreaser, or use cotton swabs and alcohol.
- Vacuum the dust with a computer vacuum cleaner to prevent the fan from being clogged.

Attention during use:

- Do not use this product near water.
- Do not spill water or any other liquids on this product.
- Do not place heavy objects on the top of this product.

Anti-static precautions

- Wear an anti-static wrist strap to avoid electrostatic discharge.
- Place the PCB on an anti-static kit or mat.
- Hold the edges of PCB when handling.
- Touch the edges of non-metallic components of the product instead of the surface of the PCB.
- Ground yourself by touching a grounded conductor or a grounded bit of metal frequently to discharge any static.

There is danger of explosion if the internal lithium-ion battery is replaced by an incorrect type. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions or recycle them at a local recycling facility or battery collection point.

Warranty Policy

- **Industrial standard products:**

12-month (1-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by us, such as CPU, CPU cooler, memory, storage devices, power adapter, panel and touchscreen.

- * PRODUCTS, HOWEVER, THAT FAIL DUE TO MISUSE, ACCIDENT, IMPROPER INSTALLATION OR UNAUTHORIZED REPAIR SHALL BE TREATED AS OUT OF WARRANTY AND CUSTOMERS SHALL BE BILLED FOR REPAIR AND SHIPPING CHARGES.

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1. Models and Attentions

1.1 Models

This manual is applied to following models:

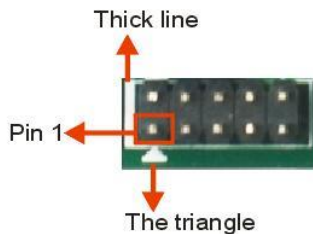
Model	CPU	COM	LAN	HDMI	VGA	LVDS/ eDP	eDP	USB	M.2 KEY-E	M.2 KEY-B	SATA 3.0
-	N100	6	1	1	1	LVDS	1	10	PCIE +UAB2.0	PCIE x1 /SATA	1
MI8385	N50	6	1	1	1	LVDS	1	10	PCIE +UAB2.0	PCIE x1 /SATA	1
MI8380	i3-N300	6	1	1	1	LVDS	1	10	PCIE +UAB2.0	PCIE x1 /SATA	1
-	N97	6	1	1	1	LVDS	1	10	PCIE +UAB2.0	PCIE x1 /SATA	1
-	x7425E	6	1	1	1	LVDS	1	10	PCIE +UAB2.0	PCIE x1 /SATA	1

1.2 Attentions

1) Notes under a table or figure indicate the difference of models, or alternative definition of specific pin of the header (jumper/connector).

2) How to identify the first pin of a header or jumper

- Usually, there is a thick line or a triangle near the header's or jumper's pin 1.



- Square pad, which you can find on the back of the motherboard, is usually used for pin 1.



3) Some models is reserved for the futur. (no P/N yet attributed)

2. General Specifications

Model		MI8380	MI8385	minimum order required		
				-	-	-
CPU	Model	Intel® Core™ Processor i3-N300	Intel® Processor N50 N100 N97			Intel® Atom® Processor x7425E
	Clock Speed	up to 3.80G	up to 3.40G	up to 3.40G	up to 3.60G	up to 3.40G
	Multi-Core	Octa	Dual	Quad	Quad	Quad
	TDP	7W	6W	6W	12W	12W
Display	1 * HDMI (TYPE-A): max resolution up to 4096×2160@30Hz ^[1] 1 * VGA (DB15): max resolution up to 1920*1080@60Hz ^[1] 1 * LVDS/eDP (Header): LVDS max resolution up to 1920*1200@60Hz (Default) or eDP max resolution up to 4096*2160@60Hz 1 * eDP (Header): max resolution up to 4096*2160@60Hz					
Memory	Support DDR4 3200 MHz, 1 * SO-DIMM Slot, Up to 16GB					
Storage ^[2]	1 * SATA3.0 7P Connector (With 1 * SATA Power Wafer) 1 * M.2 Key-B Slot (PCIe x2/SATA, Default PCIe x1/SATA, Support PCIe x1 NVMe/SATA SSD, Auto Detect, 2242/2280)					
Ethernet	1 * Realtek GBE LAN Chip (10/100/1000 Mbps, RJ45)					
Audio	Realtek Audio codec 1 * Line-Out + MIC 2in1 3.5mm Jack (Default CTIA, OMTPEL SEL by res) 1 * R/L Amplifier Wafer, 3-W (per channel) into an 8-Ω Loads					
Expansion Slot	1 * M.2 Key-E Slot (PCIe+USB2.0, Support WIFI+BT, 2230) ^[3]					
COM	1 * RS232 (COM1, DB9M/ Header, Full Lanes) ^[5] 3 * RS232 (COM2-4, Header, Full Lanes) 2 * RS232 (COM5-6, Header, Two Lanes)					
USB	4 * USB3.0 (TYPE-A, Rear IO) 2 * USB2.0 (TYPE-A, Rear IO) ^[1] 4 * USB2.0 (Header, Internal) ^[4] 1 * USB2.0 (Wafer, Internal) ^{[3] [4]}					
Other Ports	1 * Parallel Jumper 1 * Cash Drawer Wafer 1 * 8-bit GPIO Wafer 1 * Front Panel Header 1 * I2C Touch Wafer 1 * System FAN Wafer 1 * CPU FAN Wafer 1 * Case Open Header 1 * CMOS Clear Jumper 1 * AT or ATX Select Jumper 1 * CMOS Clear Jumper 1 * Power Debug Wafer					
System	Windows 10 IoT Enterprise 2021 LTSC, Windows 10 (21H2), Windows 11 (21H2) or later, Linux Kernel 5.17 or later					
Temperature	Storage: -20~75°C Operating: 0~60°C					

BIOS	AMI UEFI BIOS (Support Watchdog Timer)
Power Supply	DC12V 1 * DC 12V Power Input Φ 2.5mm Jack (Mini-din 4P Jack Optional) 1 * ATX 4P Power Input Connector (Wafer Optional) 1 * DC 12V+5V Power Output Wafer
Factor	170mm*170mm

Notes:

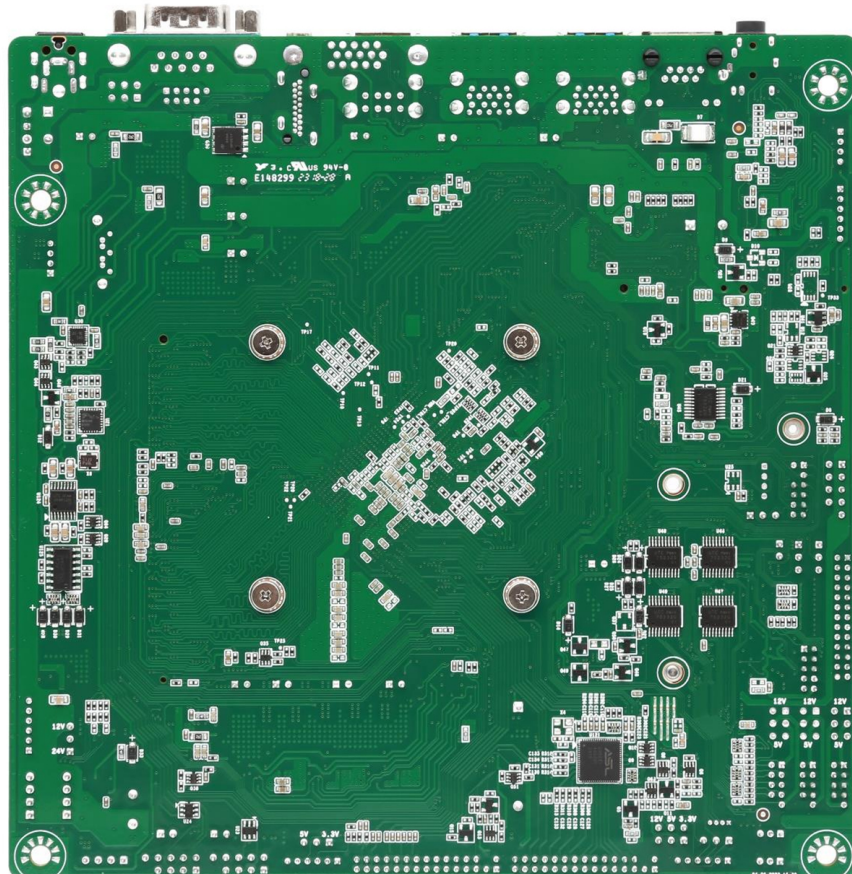
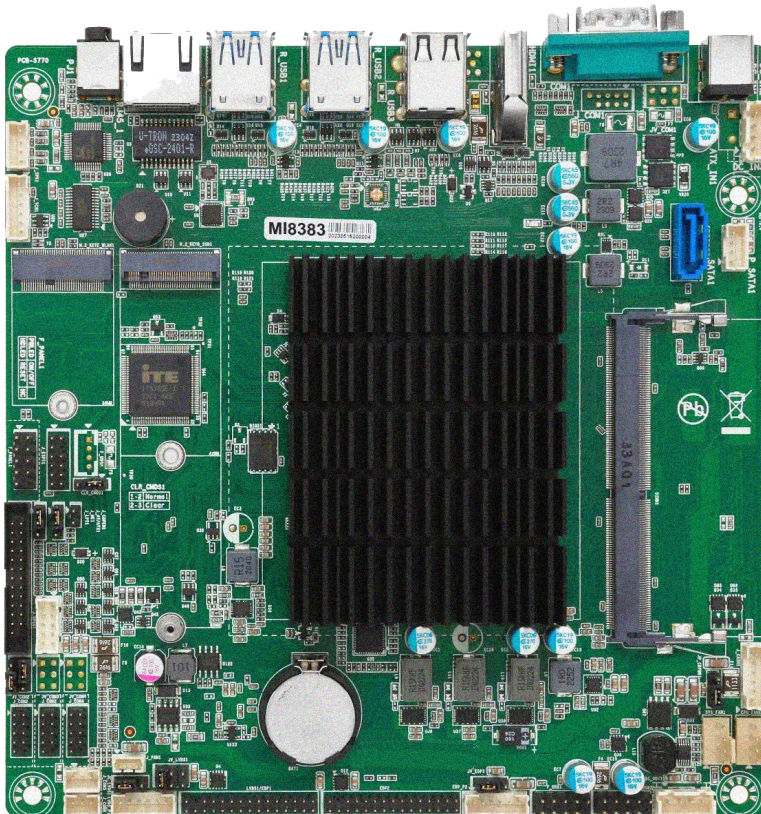
[1]: VGA1 and HDMI1+R_USB3(Mark 26) on rear I/O share the same position and are mutually exclusive. They can't be selected simultaneously. (BOM selectable)

[2]: SATA signal of SATA1 colay with one of PCIE signal for M.2_KEYB_SSD1. (BOM selectable)

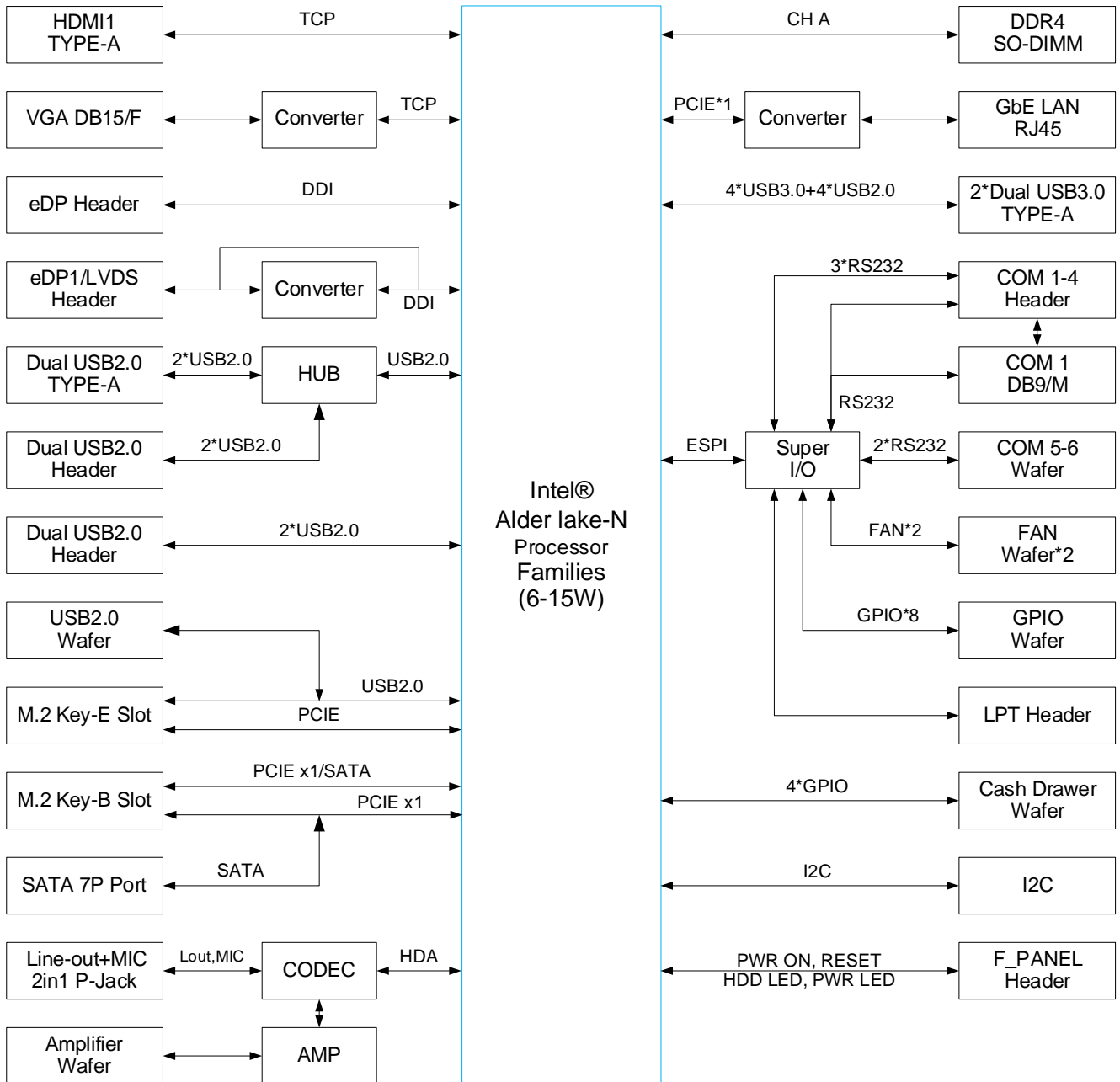
[3]: USB2.0 signal of M.2_KEYE_WLAN1 colay with F_USB3 (Mark 27), they can't be selected simultaneously. (BOM selectable)

[4]: USB2.0 signal of F_USB2 and R_USB3 (mark 26) come from the same HUB IC. When R_USB3 is't used, this interface can be deleted.

[5]: COM1 (Mark 28) and J_COM1 (Mark 29) use the same signal. They cannot be used simultaneously. (BOM selectable)



3. Functional Block Diagram



Jumpers / Headers and Connectors


①	U1	CPU
②	DIMM1	DDR4 SO-DIMM Slot
③	DC_IN1 (DC_IN2)	DC 12V Power Input Φ 2.5mm Jack (DC 12V Power Input Mini-din 4P Jack)
④	ATX_IN1 (DC_IN3)	ATX 4P Power Input Connector (DC 12V Power Input Wafer)
⑤	DC_OUT1 (DC_OUT1_PATCH1)	DC 12V+5V Power Output Wafer
⑥	HDMI1	HDMI TYPE-A Connector
⑦	VGA1	VGA DB15/F Connector
⑧	LVDS1/EDP1	eDP/LVDS Signal Header
⑨	LVDS_P1	eDP/LVDS Backlight Control Wafer
⑩	JV_LVDS1	LVDS VDD Select Jumper
⑪	JC_LVDS1	LVDS Backlight PWM/CCFL Select Jumper
⑫	EDP2	eDP Signal Header
⑬	EDP_P2	eDP Backlight Control Wafer
⑭	JV_EDP2	eDP VDD Select Jumper
⑮	PJ1	Line-Out + MIC 2in1 3.5mm Jack
⑯	J_SPK1	L/R Amplifier Wafer
⑰	SATA1	SATA3.0 7P Connector
⑱	P_SATA1	SATA Power Wafer
⑲	M.2_KEYB_SSD1	M.2 Key-B Slot (PCIe x2/SATA, Support PCIe x2 NVMe/ SATA SSD, Auto Detect, 2242/2280)
⑳	M.2_KEYE_WLAN1	M.2 Key-E Slot (PCIe+USB2.0, Support WIFI+BT, 2230)
㉑	RJ45_1	GBE LAN RJ45 Connector
㉒	R_USB1	Dual USB3.0 TYPE-A Connector
㉓	R_USB2	Dual USB3.0 TYPE-A Connector
㉔	F_USB1	Front Dual USB2.0 Header
㉕	F_USB2	Front Dual USB2.0 Header
㉖	R_USB3	Dual USB2.0 TYPE-A Connector
㉗	F_USB3	Front USB2.0 Wafer
㉘	COM1	COM1 DB9M Connector
㉙	J_COM1	COM1 Header
㉚	JV_COM1	COM1 Pin1/PIN9 VDD Select Jumper
㉛	J_COM2	COM2 Header
㉜	JV_COM2	COM2 Pin1/PIN9 VDD Select Jumper
㉝	J_COM3	COM3 Header
㉞	JV_COM3	COM3 Pin1/PIN9 VDD Select Jumper
㉟	J_COM4	COM4 Header
㊱	JV_COM4	COM4 Pin1/PIN9 VDD Select Jumper

37	J_COM5	COM5 Wafer
38	J_COM6	COM6 Wafer
39	J_LPT1	Parallel Header
40	J_CASH1	Cash Drawer Wafer
41	JP_CDPWR1	Cash Drawer VDD Select Jumper
42	J_GPIO1	GPIO Wafer
43	F_PANEL1	Front Panel Header
44	J_TCH1	I2C Touch Wafer
45	SYS_FAN1	System FAN Wafer
46	CPU_FAN1	CPU FAN Wafer
47	J_COPEN1	Case Open Header
48	BAT1	CMOS Battery
49	CLR_CMOS1	CMOS Clear Jumper
50	J_AT/ATX1	AT or ATX Mode Select Jumper
51	J_ME1	ME Flash Jumper
52	J_ESPI1	ESPI Debug Header
53	BZ1	Buzzer
54	J_PRM1	Power Debug Wafer


6. Definition of Jumpers / Headers and Connectors

1) Mark No.4 ATX_IN1/DC_IN3

ATX_IN1 (ATX 4P Power Input Connector)


Graphic	Pin	Definition	Pin	Definition
	1	GND	3	VCC12
	2	GND	4	VCC12

DC_IN3 (DC 12V Power Input Wafer 4*1 Pin 2.54mm)


Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	VCC12	4	GND

2) Mark No.5 DC_OUT1/DC_OUT1_PATCH1

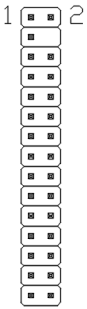
DC_OUT1/ (DC 12V+5V Power Output Wafer 4*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5

DC_OUT1_PATCH1 (DC 12V+5V Power Output Wafer 4*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5


3) Mark No.8 LVDS1/EDP1 (eDP/LVDS Signal Header 15*2 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL [1]	2	VDD_PANEL [1]
	3	VDD_PANEL [1]		
	5	LVDS_PRSENT# /EDP1_HPDP	6	LVDS_PRSENT# /EDP1_HPDP
	7	LVDS_A_DATA0-	8	LVDS_A_DATA0+
	9	LVDS_A_DATA1-	10	LVDS_A_DATA1+
	11	LVDS_A_DATA2-	12	LVDS_A_DATA2+
	13	GND	14	GND
	15	LVDS_A_CLK-	16	LVDS_CLKA+
	17	LVDS_A_DATA3-	18	LVDS_A_DATA3+
	19	LVDS_B_DATA0- /EDP1_TX0- [2]	20	LVDS_B_DATA0+ /EDP1_TX0+ [2]
	21	LVDS_B_DATA1- /EDP1_TX1- [2]	22	LVDS_B_DATA1+ /EDP1_TX1+ [2]
	23	LVDS_B_DATA2- /EDP1_TX2- [2]	24	LVDS_B_DATA2+ /EDP1_TX2+ [2]
	25	GND	26	GND
	27	LVDS_B_CLK- /EDP1_TX3- [2]	28	LVDS_B_CLK+ /EDP1_TX3+ [2]
29	LVDS_B_DATA3- /EDP1_AUX- [2]	30	LVDS_B_DATA3+ /EDP1_AUX+ [2]	


Notes:

- [1]: Panel Power VDD is 3.3V by default, 5V/12V is selectable by “LVDS VDD Select Jumper” (JV_LVDS1, Mark 10).
- [2]: It supports LVDS by default and can support eDP if specified. (resistor selectable)


4) Mark No.9 LVDS_P1 (eDP/LVDS Backlight Control Wafer 6*1 Pin 2.00mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	LVDS_BKLT_EN
	2	GND	5	VCC12
	3	LVDS_BKLT_CTL	6	VCC12

5) Mark No.10 JV_LVDS1 (LVDS VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	VCC3.3
	3-4	VCC5
	5-6	VCC12

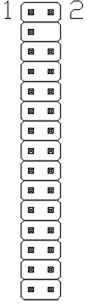
6) Mark No.11 JC_LVDS1 (LVDS Backlight PWM/CCFL Select Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	Controlled by PWM
	2-3	Controlled by CCFL [1]

Notes:

[1]: Controlled by CCFL by default, PWM# optional. (resistor selectable)


7) Mark No.12 EDP2 (eDP Signal Header 15*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL2 [1]	2	VDD_PANEL2 [1]
	3	VDD_PANEL2 [1]		
	5	EDP2_HPD	6	EDP2_HPD
	7	N/C	8	N/C
	9	N/C	10	N/C
	11	N/C	12	N/C
	13	GND	14	GND
	15	N/C	16	N/C
	17	N/C	18	N/C
	19	EDP2_TX0-	20	EDP2_TX0+
	21	EDP2_TX1-	22	EDP2_TX1+
	23	EDP2_TX2-	24	EDP2_TX2+
	25	GND	26	GND
	27	EDP2_TX3-	28	EDP2_TX3+
	29	EDP_AUX-	30	EDP_AUX+


Notes:

[1]: Panel Power VDD is 3.3V by default, 5V is selectable by “eDP VDD Select Jumper” (JV_EDP2, Mark 14).


8) Mark No.13 EDP_P2 (eDP Backlight Control Wafer 6*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	LVDS_BKLT_EN
	2	GND	5	VCC12
	3	EDP2_BKLT_CTL	6	VCC12


9) Mark No.14 JV_EDP2 (eDP VDD Select Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	VCC3.3
	2-3	VCC5

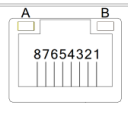
10) Mark No.16 J_SPK1 (L/R Amplifier Wafer 4*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	SPK_OUT_L-	3	SPK_OUT_R-
	2	SPK_OUT_L+	4	SPK_OUT_R+

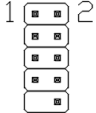
11) Mark No.18 P_SATA1 (SATA Power Wafer 4*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5

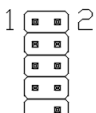
12) Mark No.21 RJ45_1 (GBE LAN RJ45 Connector)

Graphic	Pin	Definition	Pin	Definition
	1	XMDI0+	5	XMDI2-
	2	XMDI0-	6	XMDI1-
	3	XMDI1+	7	XMDI3+
	4	XMDI2+	8	XMDI3-
	A	Active LED	ACT: Twinkling Yellow Only LINK: Lights Off Stop: Lights Off	B
				1000M: Turn Yellow 100M: Turn Green 10M: Lights Off


13) Mark No.24 F_USB1 (Front USB2.0 Header 5*2 Pin 2.54 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	2	VCC5
	3	USB2.0_1-	4	USB2.0_2-
	5	USB2.0_1+	6	USB2.0_2+
	7	GND	8	GND
			10	GND

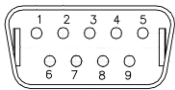
14) Mark No.25 F_USB2 (Front USB2.0 Header 5*2 Pin 2.54 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	2	VCC5
	3	USB2.0_1-	4	USB2.0_2-
	5	USB2.0_1+	6	USB2.0_2+
	7	GND	8	GND
	9		10	GND

15) Mark No.27 F_USB3 (Front USB2.0 Wafer 4*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC5	3	USB2.0+
	2	USB2.0-	4	GND

16) Mark No.28 COM1 (COM1 DB9M Connector)

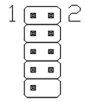
Graphic	Pin	Definition	Pin	Definition
	1	PIN1 ^[1]	6	DSR
	2	RXD	7	RTS
	3	TXD	8	CTS
	4	DTR	9	PIN9 ^[2]
	5	GND		

Notes:

[1]: Pin1 of COM1 can be 5V or 12V, selected by “COM1 Pin1/PIN9 VDD Select Jumper” (JV_COM1, Mark 30). When deleting JV_COM1 and change circuit, Pin1 of COM1 can also be DCD.

[2]: Pin9 of COM1 can be 5V or 12V, selected by “COM1 Pin1/PIN9 VDD Select Jumper” (JV_COM1, Mark 30). When deleting JV_COM1 and change circuit, Pin9 of COM1 can also be RI.

17) Mark No.29 J_COM1 (COM1 Header 5*2 Pin 2.00 mm)


Graphic	Pin	Definition	Pin	Definition
	1	PIN1 [1]	2	RXD
	3	TXD	4	DTR
	5	GND	6	DSR
	7	RTS	8	CTS
	9	PIN9 [2]		

Notes:

[1]: Pin1 of COM1 can be 5V or 12V, selected by “COM1 Pin1/PIN9 VDD Select Jumper” (JV_COM1, Mark 30). When deleting JV_COM1 and change circuit, Pin1 of COM1 can also be DCD.

[2]: Pin9 of COM1 can be 5V or 12V, selected by “COM1 Pin1/PIN9 VDD Select Jumper” (JV_COM1, Mark 30). When deleting JV_COM1 and change circuit, Pin9 of COM1 can also be RI.

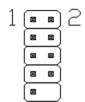
18) Mark No.30 JV_COM1 (COM1 Pin1/PIN9 VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-3,2-4(Default)	PIN1_COM1: VCC12 PIN9_COM1: VCC12
	3-5, 4-6	PIN1_COM1: VCC5 PIN9_COM1: VCC5

Notes:

*: Jumper 1-3/3-5 select the COM1_PIN1 signal. Jumper 2-4/4-6 select the COM1_PIN9 signal.

19) Mark No.31 J_COM2 (COM2 Header 5*2 Pin 2.00 mm)


Graphic	Pin	Definition	Pin	Definition
	1	COM2_PIN1 [1]	2	COM2_RXD
	3	COM2_TXD	4	COM2_DTR
	5	GND	6	COM2_DSR
	7	COM2_RTS	8	COM2_CTS
	9	COM2_PIN9 [2]		

Notes:

[1]: Pin1 of COM2 can be 5V or 12V, selected by “COM2 Pin1/PIN9 VDD Select Jumper” (JV_COM2, Mark 32). When deleting JV_COM2 and change circuit, Pin1 of COM2 can also be DCD.

[2]: Pin9 of COM2 can be 5V or 12V, selected by “COM2 Pin1/PIN9 VDD Select Jumper” (JV_COM2, Mark 32). When deleting JV_COM2 and change circuit, Pin9 of COM2 can also be RI.

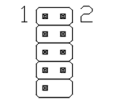
20) Mark No.32 JV_COM2 (COM2 Pin1/PIN9 VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-3,2-4(Default)	PIN1_COM2: VCC12 PIN9_COM2: VCC12
	3-5, 4-6	PIN1_COM2: VCC5 PIN9_COM2: VCC5

Notes:

*: Jumper 1-3/3-5 select the COM2_PIN1 signal. Jumper 2-4/4-6 select the COM2_PIN9 signal.

21) Mark No.33 J_COM3 (COM3 Header 5*2 Pin 2.00 mm)


Graphic	Pin	Definition	Pin	Definition
	1	PIN1 [1]	2	RXD
	3	TXD	4	DTR
	5	GND	6	DSR
	7	RTS	8	CTS
	9	PIN9 [2]		

Notes:

[1]: Pin1 of COM3 can be 5V or 12V, selected by “COM3 Pin1/PIN9 VDD Select Jumper” (JV_COM3, Mark 34). When deleting JV_COM3 and change circuit, Pin1 of COM3 can also be DCD.

[2]: Pin9 of COM3 can be 5V or 12V, selected by “COM3 Pin1/PIN9 VDD Select Jumper” (JV_COM3, Mark 34). When deleting JV_COM3 and change circuit, Pin9 of COM3 can also be RI.

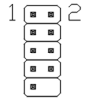
22) Mark No.34 JV_COM3 (COM3 Pin1/PIN9 VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-3,2-4(Default)	PIN1_COM3: VCC12 PIN9_COM3: VCC12
	3-5, 4-6	PIN1_COM3: VCC5 PIN9_COM3: VCC5

Notes:

*: Jumper 1-3/3-5 select the COM3_PIN1 signal. Jumper 2-4/4-6 select the COM3_PIN9 signal.

23) Mark No.35 J_COM4 (COM4 Header 5*2 Pin 2.00 mm)


Graphic	Pin	Definition	Pin	Definition
	1	PIN1 [1]	2	RXD
	3	TXD	4	DTR
	5	GND	6	DSR
	7	RTS	8	CTS
	9	PIN9 [2]		

Notes:

[1]: Pin1 of COM4 can be 5V or 12V, selected by “COM4 Pin1/PIN9 VDD Select Jumper” (JV_COM4, Mark 36). When deleting JV_COM4 and change circuit, Pin1 of COM4 can also be DCD.

[2]: Pin9 of COM4 can be 5V or 12V, selected by “COM4 Pin1/PIN9 VDD Select Jumper” (JV_COM4, Mark 36). When deleting JV_COM4 and change circuit, Pin9 of COM4 can also be RI.


24) Mark No.36 JV_COM4 (COM4 Pin1/PIN9 VDD Select Jumper 3*2 Pin 2.54 mm)

Graphic	Setting	Function
	1-3,2-4(Default)	PIN1_COM4: VCC12 PIN9_COM4: VCC12
	3-5, 4-6	PIN1_COM4: VCC5 PIN9_COM4: VCC5


Notes:

*: Jumper 1-3/3-5 select the COM4_PIN1 signal. Jumper 2-4/4-6 select the COM4_PIN9 signal.

25) Mark No.37 J_COM5 (COM5 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		


26) Mark No.38 J_COM6 (COM6 Wafer 3*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	RXD	3	GND
	2	TXD		

27) Mark No.39 J_LPT1 (Parallel Jumper 13*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	STB#	2	AFD#
	3	PD0	4	ERR#
	5	PD1	6	INIT#
	7	PD2	8	SLIN#
	9	PD3	10	GND
	11	PD4	12	GND
	13	PD5	14	GND
	15	PD6	16	GND
	17	PD7	18	GND
	19	ACK#	20	GND
	21	BUSY	22	GND
	23	PE	24	GND
	25	SLCT	26	N/C


28) Mark No.40 J_CASH1 (Cash Drawer Wafer 6*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_CASH [1]	4	GND
	2	CASH1_CTRL	5	CASH2_CTRL
	3	CASH1_DEC	6	CASH2_DEC

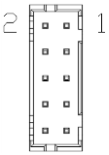
Notes:

[1]: CASH VDD is 24V by default, 12V is selectable by “Cash Drawer VDD Select Jumper” (JP_CDPWR1, Mark 41).

29) Mark No.41 JP_CDPWR1 (Cash Drawer VDD Select Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	VCC24
	3-4	VCC12

30) Mark No.42 J_GPIO1 (GPIO Wafer 5*2 Pin 2.00 mm)

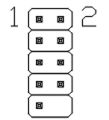
Graphic	Pin	Definition	Pin	Definition
	1	SIO_GPI11 (0xA00 Bit1, H ^[1])	2	SIO_GPI15 (0xA00 Bit5, H ^[1])
	3	SIO_GP16 (0xA00 Bit6, H ^[1])	4	SIO_GP33 (0xA02 Bit3, H ^[1])
	5	SIO_GP47 (0xA03 Bit7, H ^[1])	6	SIO_GP50 (0xA04 Bit0, H ^[1])
	7	SIO_GP64 (0xA05 Bit4, H ^[1])	8	SIO_GP65 (0xA05 Bit5, H ^[1])
	9	GND	10	VCC_GPIO ^[2]

Notes:


[1]: "H" or "L" means the default voltage is High or Low level (5V GPIO).

[2]: Power on this Pin is 5V by default, 3.3V is available if specified. (resistor selectable)


31) Mark No.43 F_PANEL1 (Front Panel Header 5*2 Pin 2.54 mm)

Graphic	Pin	Definition	Pin	Definition
	1	HDD_LED+	2	PWR_LED+
	3	HDD_LED-	4	PWR_LED-
	5	RESET-	6	PWR+
	7	RESET+	8	PWR-
	9	N/C	10	


32) Mark No.44 J_TCH1 (I2C Touch Wafer 6*1 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	VCC3.3	4	I2C_RST
	2	GND	5	I2C_SCL
	3	I2C_INT	6	I2C_SDA


33) Mark No.45 SYS_FAN1 (System FAN Wafer 4*1 Pin 2.54 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC12	4	FAN Speed Control


34) Mark No.46 CPU_FAN1 (CPU FAN Wafer 4*1 Pin 2.54mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC12	4	FAN Speed Control


35) Mark No.47 J_COPEN1 (Case Open Header 2*1 Pin 2.54mm)

Graphic	Setting	Function
	1-2: Connected	Active Case Open
	1-2: Open	Normal


36) Mark No.49 CLR_CMOS1 (CMOS Clear Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	Normal
	2-3	Clear CMOS

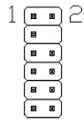
37) Mark No.50 J_AT/ATX1 (AT/ ATX Select Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	ATX MODE
	2-3	AT MODE

38) Mark No.51 J_ME1 (ME Flash Jumper 3*1 Pin 2.54 mm)

Graphic	Setting	Function
	1-2(Default)	ME Protect
	2-3	ME Programmable


39) Mark No.52 J_ESPI1 (ESPI Debug Header 6*2 Pin 2.00 mm)

Graphic	Pin	Definition	Pin	Definition
	1	ESPI_IO0	2	VCC3.3
	3	ESPI_IO1		
	5	ESPI_IO2	6	ESPI_CLK
	7	ESPI_IO3	8	GND
	9	ESPI_CS0-	10	VCC3.3
	11	ESPI_ALERT0_N	12	PLTRST_N ^[1]

Notes:

[1]: Signal on this Pin is PLT_RST_N by default, ESPI_RST0_N is available if specified. (resistor selectable).

40) Mark No.54 J_PRM1 (Power Debug Wafer 4*1 Pin 1.25 mm)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	VCCIN_SCL
	2	IMVP_PE	4	VCCIN_SDA

7. BIOS setup

Available separately

【End】